TEMPERATURE AND FREQUENCY DEPENDENCIES OF CHARGING AND DISCHARGING PROPERTIES IN MOS MEMORY BASED ON NANOCRYSTALLINE SILICON DOT

Shaoyun Huang, Souri Banerjee, and Shunri Oda
Research Center for Quantum Effect Electronics, Tokyo Institute of Technology,
2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552, JAPAN

ABSTRACT

Temperature and frequency dependencies of the electrical properties of SiO2/nanocrystalline Si (nc-Si)/SiO2 sandwich structures have been studied. A clear positive shift in capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics suggests electron trapping in nc-Si dots. The role of interface states and deep traps in these devices has also been examined, which shows that they have little effect on the overall device performance.

INTRODUCTION

In our previous report [1], it was pointed out that electron charging and discharging processes in metal-oxide-semiconductor field-effect transistor (MOSFET) memory structures based on silicon quantum dots can be accurately detected by capacitance-voltage (C-V) and conductance-voltage (G-V) techniques. In this work, we will focus on the temperature and frequency dependencies of C-V and G-V measurements, which reveal the role of defects in the structure. Although much work has been devoted to fabricate ideal memory structures and to obtain reproducible hysteresis in the current-voltage (I-V) characteristics [2,3], the retention mechanism associated with interface defects is still not clear. Kohno et al. investigated the transient current of a Si quantum dot floating gate MOS structure and showed a charging and discharging process. However, effects of interface defects were not apparent in their study [4]. On the other hand, Shi et al. claimed that deep level defects would often result in long-term retention behavior [5], whereas, Hinds et al. concluded that interface defects did not play a dominant role in charge retention mechanism in MOSFET memory devices [6]. Hence further study on the retention mechanism in relation to interface defects would be helpful as it generally has a large influence on overall device performance.

EXPERIMENTAL DETAILS

The memory device investigated in the present report is a SiO2/nanocrystalline Si (nc-Si) dot/ SiO2 sandwich diode structure on an n-type silicon substrate. For comparison, control samples having similar structure but without nc-Si dots were also prepared. The detailed fabrication processes of such a device have been described elsewhere [1].

The electrical properties of this sandwich structure device were measured by HP4156B precision semiconductor parameter analyser and HP 4284A precision LCR meter in the temperature range between 30 K and room temperature.
A typical memory device sample consists of nc-Si dots \((1.4 \times 10^{11}/\text{cm}^2)\) with 8 nm diameter, sandwiched between a 2 nm thick tunnel oxide layer and a 54 nm thick upper gate oxide layer. The capacitor surface portion covered by Si dots is about 10 \(\%\).

The memory electrical characteristics of C-V and G-V shown in Fig. 1 were obtained by sweeping the voltage between inversion and accumulation regions at room temperature.

![Figure 1](image-url)

**Figure 1** Typical C-V and G-V characteristics obtained by sweeping gate voltage between \(-5\) V and 1 V. The peak position in the G-V characteristics is around the flat-band voltage.

Compared to the control sample, where no hysteresis in C-V or G-V characteristics and conductance peak in G-V characteristics could be found, the above hysteresis and peak shift can be attributed to electron traps in the sandwiched nc-Si or at the interfaces of the nanocrystal dots but not to states in the oxide matrix or at the Si substrate/tunnel oxide interface. Both the magnitude of hysteresis in C-V and the shift in the peak positions in G-V are about 0.12 V. It is worthwhile to note that no holes were trapped at the inversion state in our experiments.

For a better understanding of the results obtained from C-V and G-V measurements, the frequency dependence of capacitance and conductance was also investigated at various temperatures, as shown in Fig. 2 and Fig. 3.

In frequency dependent measurements at room temperature, Fig. 2, we found similar clockwise C-V hysteresis (Fig. 2a) and a constant full width at half maximum (FWHM) of the peaks in G-V characteristics (Fig. 2b) in the frequency range of 10 kHz to 1 MHz, which suggest that hysteresis and conductance peak come from the same origin [7]. Moreover, there is no dispersion or stretchout in the C-V characteristics along the gate voltage axis for the entire experimental frequency range observed in C-V characteristics even at 30 K, which is consistent with the fact that the C-V hysteresis and G-V peak are not due to interface traps, as they generally give rise to time- or frequency-dependent C-V or G-V characteristics [8]. However, small but noticeable shifts in conductance peaks with frequency as well as temperature have been observed in the G-V characteristics (Fig. 2b and Fig. 3b). These may be explained by the fact that the conductance is related directly to the energy loss provided by the ac signal source during capture and emission of carriers by nc-Si dots, making the measurement of equivalent parallel conductance more sensitive and accurate.
Figure 2 (a) C-V characteristics measured at 300 K for various frequencies. (b) G-V characteristics measured at same conditions.

For the temperature-dependent measurements at a given frequency (1 MHz), a similar clockwise hysteresis in the C-V characteristics and the FWHM of the conductance peak in G-V characteristics was also found as shown in Fig. 3. In this case, a perceptible right-hand shift along the gate voltage axis with decreasing temperature occurred in C-V characteristics. A small right-hand shift in the peak position was also found in G-V characteristics with decreasing temperature. These results can be compared with that of frequency dependent measurements, which will be discussed later in detail.
Figure 3 (a) C-V characteristics measured at 1 MHz for various temperatures. (b) G-V measurements measured at same conditions.

In order to investigate the influence of interface states, we plot the conductance peak value as a function of reciprocal temperature in Fig. 4. A very weak temperature dependence of the conductance has been noted and an activation energy as small as 5 meV has been derived, within the experimental error at 1 MHz and 50 kHz.

Figure 4 Conductance peak value ($G_m$) vs. reciprocal temperature measurement at (a) 1 MHz and (b) 50 kHz. The estimated activation energies are (a) 4.8 meV and (b) 2.3 meV.
DISCUSSION

Our experimental results suggest that, at sufficient negative voltage (erasing voltage), no electron resides in the nc-Si dots and that there is no hole trapping in nc-Si dots (as mentioned before), i.e. a neutral charge state is maintained. When voltage is swept to a large positive value, a number of electrons will be stored in nc-Si dots by direct tunneling process through the ultrathin oxide, resulting in the shift in capacitance as well as conductance characteristics. In the G-V measurements, nc-Si dot trap levels are detected through the ac loss resulting from changes in their occupancy produced by small variations of gate voltage [8]. A small ac voltage applied to the gate of an MOS capacitor alternately moves the band edges toward or away from the Fermi level. Majority carriers are captured or emitted, changing the occupancy of nc-Si dots energy levels in a small energy interval of a few \( kT/e \) widths, where \( k \), \( T \) and \( e \) are the Boltzmann constant, absolute temperature and elementary charge, respectively. The capture and emission of majority carrier cause an energy loss observed at all frequencies. For a given ac frequency in our experiment the gate voltage was varied from accumulation to depletion state. In the accumulation state, majority carrier density is very large near the Si-SiO\(_2\) interface, so that the nc-Si dot capture rates are very high compared to the ac frequency. Nanocrystalline-Si dot levels respond immediately to the ac voltage, and no loss is observed. In the depletion state, majority carrier density at the Si-SiO\(_2\) interface is reduced. As a result, capture rates become comparable to the ac frequency, leading to significant loss. Further in the depletion state, near midgap, majority carrier density becomes so low that nc-Si dot levels hardly respond. In such a case, the capture rate is also low so that almost no carriers are exchanged between the nc-Si dots and the silicon, resulting in a lower loss. This could be the reason for the appearance of a single conductance peak around flat-band voltage. It should be emphasized that the occurrence of the conductance peak observed in our experiments should be associated with the ac loss due to the capture and emission of electrons by the nc-Si dots but not to the Si substrate/tunnel oxide interface states [9,10], a conclusion drawn from a comparison with the experimental observation with the control sample without nc-Si dots.

As noted in Fig. 2a, the magnitude of hysteresis and the value of the threshold voltage remained almost unchanged with varying frequency, whereas the conductance peaks shifted monotonically to the left with decreasing frequency (Fig. 2b). This may be attributed to the response in change of charge in interface states. At a given frequency, all traps with time constants shorter than the reciprocal of the frequency respond to the measuring signal and the flat-band voltage will be reached at a particular value of voltage. At a lower frequency, however, slower traps can respond. As a result of which, previously trapped charges would be discharged. Hence, the flat-band voltage will be reached at a lower gate voltage. For comparison, a stretchout in C-V curves and a left-hand shift in conductance peak were observed in Fig. 3a and Fig. 3b, respectively. Several interesting features can be noted. The stretch about the gate voltage axis is due to the response of the interface traps to the applied dc voltage. Both stretchout in C-V and shift in G-V curves can be explained by the change of electrons frozen in interface traps at low temperature, where frozen charge in interface states cannot contribute to the total capacitance or to screening gate voltage.

Another way to find the nature of interface states in these kinds of devices is through the estimation of the thermal activation energy [8]. In Fig. 4, a very weak temperature dependence of conductance and an absence of activation have been observed, which indicate that deep defect have negligible contribution in the charging and discharging processes in nc-Si dots. However it
is likely that the shallow interface states near the edge of conductance band, probably, result in the stretchout in C-V characteristics and shift in G-V characteristics [11], as observed in our present samples. Thus, it can be concluded that in the present case the device performance depends only on the nc-Si dots sandwiched between SiO₂ layers.

To explain the observed charging and discharging behaviors of nc-Si dots, Shi et al. suggested that electrons should not reside in the conduction band but in nc-Si related deep level traps [5]. According to the model, the retention time should be thermally activated at deep trap energy level. However, in their experiments the charge-loss rate only decreased slightly as the temperature was decreased from 300 to 80 K. Our frequency- and temperature-dependent results also indicate that neither interface defect nor deep defect is dominant for the charging or discharging processes in our samples. It is relevant to mention that unlike the samples investigated by Shi et al., the samples in our experiments are free of plasma damage owing to the fabrication technique discussed in the previous paper [1]. Therefore, the chances of incorporation of deep defects are further reduced, which is consistent with the experimental results. Hence an alternative model, which is not associated with interface defects, should be developed to explain the long-term retention behavior observed in our experiments.

CONCLUSION

We prepared SiO₂/nc-Si/SiO₂ sandwich structure memory devices. Sensitive electrical measurements of C-V and G-V were utilized to investigate the charging and discharging in nc-Si dots. Experiments show that neither interface defect nor deep defect is dominant for the charging and discharging of the dots. An alternative model, which does not invoke interface defects, should be developed to explain the long-term retention behavior.

ACKNOWLEDGEMENTS

The authors would like to thank Dr. K. Arai and J. Oomachi for their help with the nc-Si dots deposition processes. Funding was supported by a grant-in aid for Scientific Research from the Ministry of Education and by the Core Research for Evolutional Science and Technology (CREST) program of the Japan Science and Technology Corporation (JST).

REFERENCES