Charge Storage Mechanism in Nano-Crystalline Si Based Single-Electron Memories

Bruce J. Hinds, Takayuki Yamanaka, and Shunri Oda
Research Center for Quantum Effect Electronics
Tokyo Institute of Technology
2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552 Japan

ABSTRACT

A memory device sensitive to a single electron stored in a nanocrystalline Si dot has been synthesized allowing for the study of charge retention lifetime. A 50 nm by 20 nm transistor channel is synthesized by E-beam lithography followed by reactive ion etching of thin (20nm) Silicon-on-Insulator (SOI) channel. This small area of the narrow channel allows for the isolation of a single nano-crystalline Si dot and elimination of channel percolation paths around the screening charge. Remote Plasma Enhanced CVD is used to form 6±2nm diameter nc-Si dots in the gas phase from a pulsed SiH4 source. Electrons stored in a dot results in an observed discrete threshold shift of 90 mV. Analysis of lifetime as a function of applied potential and temperature show the dot to be an acceptor site with nearly Poisson lifetime distributions. An observed 1/T^2 dependence of lifetime is consistent with a direct tunneling process, thus interface states are not the dominant mechanism for electron storage in this device structure. Median lifetimes are modeled by a direct tunneling process, which is influenced by gate bias and dot size.

INTRODUCTION

Devices sensitive to a single electron have the possibility to drastically improve memory and logic device performance by high device density and low power. With current scaling trends in metal oxide semiconductor field effect transistors (MOSFET) production there is the inevitable need to understand and optimize devices that operate with only a statistically small number of electrons whose transport is mesoscopic. Si based nanoscale devices are strong contenders due to existing Si process infrastructure as well as the nearly perfect interface between SiO2 dielectric and Si. The latter advantage is paramount to success, since single electronic devices are obviously sensitive to local and background charged defects.

Several groups have demonstrated single electron memory effects in Si systems. Examples include charge stored in nanocrystalline Si dots (nc-Si) above large area FET channel[1], charge stored in single poly-Si dot over narrow SOI channel [2-4], and memory devices based on charge through complex percolation paths of several nm thick SOI [5]. Generally there is a significant trade off between short write/erase time and long memory retention time, which is determined mainly by the tunnel oxide thickness. The write time is reported to be many orders of magnitude faster than retention time [1], which is not expected if both write and erase process are due to direct tunneling. One possible explanation for the long retention time is that stored electrons are trapped in interface states on the Si nanocrystals. The effects of interface states on single electron memory has been shown to be important after H passivation of interface states are removed by annealing, however the role of interface states in initial devices is not known [6]. By studying the lifetime of charge stored inside the dot it is possible to ascertain whether the electron is delocalized over the entire dot or localized at interface traps. However this requires
the study of a single dot since a distribution of dot sizes and complex electron percolation path in the channel would make analysis of multidot systems impossible. Reports of single electron memory using a single poly Si dot defined by twice aligned e-beam lithography focused on the self limited charging of memory and no lifetime studies are reported. However it is reasonable to expect a significant role for interface states due to the process conditions to form poly-Si dot.

Remote plasma enhanced chemical vapor deposition (RPECVD) with pulsed source reactants readily forms a single crystal nc-Si dots (8±1nm diameter) in a gas phase process [7]. The advantage of this process over other CVD processes is that spherical dots with good passivation and small size dispersion are formed without the co-deposition of amorphous-Si, which can act as charged defect sites. Although the exact location of deposited nc-Si is not controlled, by making a channel with a small active area we can statistically isolate a device where a single nc-Si dot determines the memory state. Presented here are the results of memory lifetime analysis as a function of temperature and applied gate bias, which show that interface traps do not dominate retention time.

EXPERIMENTAL DETAILS

The schematic of the field effect transistor (FET) with nc-Si floating gate nodes is shown in Figure 1a. The device fabrication process begins with the dry-oxidation thinning of separation-by-implanted-oxygen (SIMOX) silicon layer to 25 nm and partial HF chemical etching of the top oxide layer. The buried oxide thickness is 400 nm. The entire wafer is lightly doped by phosphorus implanted to $4 \times 10^{17}$ cm$^{-3}$, diffusion annealed at 900 for 30min, then top oxide removed by HF etch.

Patterns (Figure 1b) for narrow Si-channels (25 nm wide and 50 nm long) are written by an electron beam (EB) lithography apparatus (JEOL JBX5(FE)). The EB process uses a RD2000N negative resist, which has high sensitivity to electron exposure and high resistance to subsequent dry etching [8]. The active area of the device results from the proportionately higher resistance due to the smaller cross sectional area of the narrow channel. Series resistance outside of gate area is reduced by using 50um wide leads. Next, electron cyclotron resonance reactive ion etching (ECR-RIE) is used to transfer the resist pattern to the SOI layer, using CF$_4$ as a reactive gas. To remove plasma damage and residual fluoride on SOI by the RIE process, 3-4 nm of the thermal oxide is grown by dry oxidation at 800°C for 20 minutes, and then removed in diluted HF (0.75%) solution. Chemical oxidation by

Figure 1. a) Schematic of single electron memory device isolating single nc-Si dot as floating gate memory node. b) Planar SEM of e-beam lithography pattern showing small active area of SOI channel.
H₂SO₄/H₂O₂ subsequently forms a 2 nm oxide tunnel barrier. Next nc-Si dots (6±2nm diameter) are deposited by RPECVD for a density of 1x10¹¹cm⁻², giving 1-2 dots in the active area. A 50 nm thick gate oxide is deposited by tetra-isocyanate silane (TICS) PECVD at 300°C. Contact pad area was heavily doped (5x10¹⁹cm⁻³) by P implant, followed by an N₂ anneal at 1000°C for 1 h. The anneal serves to improve gate oxide quality and to activate dopants. Finally, contact pads and gate electrodes are formed by the Al lift-off technique. The memory device is mounted on a probe station connected to a cryostat cooler, which permits temperature as low as 20K. A semiconductor parameter analyzer (HP4156B) and pulse generator (HPB1104A) with automated collection software is used for electrical measurement.

RESULTS AND DISCUSSION

The basis of single electron memory is to have a discrete shift in threshold voltage from the screening effect of charge stored in the dot above the conduction channel. The observed shift in V₁h of 90mV (not shown) can be expected for a single charge over a 25nm wide channel and a gate oxide thickness of 50nm. Notable is the discrete step in conduction at a constant gate bias after a writing pulse in Figure 2. A stepwise increase in conduction clearly shows the discrete emission of an electron from the nc-Si dot. It should be noted that the data shown in Figure 2 is a representative example of memory lifetime and that there was significant distribution of lifetimes for other pulses under the same conditions. Thus to have an accurate measure of the lifetime distribution it is necessary to measure lifetime using at least several hundred cycles. 

Figure 2. Time dependence of conduction after writing process. Stepwise increase in current is due to electron emission from memory node.

Figure 3. Distribution of memory lifetimes as a function of applied erase bias (front series is at Vₑ = –2.25V) at 295K. Inset shows pulse sequence. Vᵮ = 6V, Vᵢ = 0.25V, 0.1s read, 0.1s erase pulse time. 400 cycles at each Vₑ.

Figure 4. Temperature dependence of memory erase time at Vₑ = -2.25V. Shown is mean lifetime after 250 erase cycles as shown in Figure 3.
study erase time in a statistical manner, the applied pulse sequence is shown in the inset of Figure 3. The erase time is the cumulative time under erase bias pulses until there is a step increase in conductance. Figure 3 shows a histogram of memory lifetimes after 400 write/erase cycles as a function of applied erase bias. As expected the dot acts as an electron acceptor site with reduced lifetime as more negative gate bias is applied. However this effect is relatively small indicating that the electron is not likely stored in a trap since this would be sensitive to Fermi level location relative to trap level. Another important aspect of Figure 3 is that the distribution of lifetime is quite broad with the mean value being nearly equal to the standard deviation. A Poisson distribution is expected for a process with high attempt frequency but low probability of emission. Figure 4 shows that there is a very small temperature dependence on lifetime and an absence of activation energy (<0.05mV). If interface states act as electron traps then an activation energy from 50-200mV would be observed [9]. Since this is not observed we can conclude that interface traps do not dominate the memory retention mechanism. The temperature dependence of lifetime is seen be proportional to $1/T^2$ which can be explained by a direct tunneling process which depends on density of states to tunnel into $(T^{3/2})$ times thermal velocity $(T^{1/2})$.

To explain observed lifetime as a function of temperature and gate bias, a relatively simple model treating the electron as a classic charge delocalized over the entire nc-Si dot can be examined. In such a model the nc-Si dot is treated as a dielectric medium with one electron in the conduction band, which allows us to ignore electron-electron coupling. A classical treatment of electron can be used since the memory lifetime ($1-10^2$ s) is much longer than electron-wave coherence time for resonant states in nc-Si dot. Thermal equilibrium with a Boltzman distribution of electron energy over time is thus assumed.

To explain the lifetime as a function of applied gate bias, an important concept is that the electron will be attracted to the top of the dot with positive bias and be unable to tunnel into the channel. Thus the electron will have to overcome the potential within the dot to reach the bottom of the dot, where tunneling can occur. This is schematically shown in Figure 5, where $\rho$ is the electron density. The potential drop across the dot is an important parameter and the difference between dielectric constants for Si (11.9) and SiO$_2$ (3.9) must be accounted for. However the dot size is so small that the parallel plate capacitor treatment is a poor approximation and Poisson’s equation must be solved in three dimensions. The potential profile across the 3-dimensional dot was calculated numerically [10] for dielectric dots without free carriers as a function of dot diameter. The empirical fit of $df$ (‘dielectric factor’) for the potential drop across dot is shown in Equation 1 where $d$ is dot diameter, $t_{gox}$ is gate oxide thickness, and $t_{tox}$ is tunnel oxide thickness. The potential drop across the dot is increased by a factor of 1.5 to 1.7 times the infinite parallel plate model (first term of Equation 1) as dot size is decreased from 12 to 4 nm.

$$\rho \rightarrow \rho_{max}$$

Figure 5. Schematic of charge localization at the top of nc-Si dot under positive gate bias. Inset at left shows diagram of electron density $\rho$ as a function of height above channel.
For calculating the electron density at the top of the dot, an important boundary condition is that the gate bias cannot confine an electron to a length smaller than quantum confinement energy will allow. That is for a given gate bias, there is a length ($a_{crit}$) where the potential drop from applied gate bias equals quantum confinement energy. This is shown in Equation 2 where the left side is potential drop from applied bias and the right side is infinite barrier quantum confinement approximation. $V_g$ is applied gate bias, $N_i$ is quantum energy level of 1 for ground state, and $m_{eff}$ is the effective mass of the electron. $a_{crit}$ is easily solved and for typical read voltages $a_{crit}$ is ~2nm, thus the top 2nm of the nc-Si will have a uniform electron density. The maximum possible electron density ($\rho_{max}$) can be calculated since the integrated probability over the dot volume is 1 electron. This is equal to the constant electron density at the top of the dot plus the integration of exponential decrease in density from applied bias (as shown in the denominator of Equation 3). $a_{crit}(V_g)$ is the critical length from Eq. 2 at a given gate bias $V_g$, $x$ is vertical distance from top of dot minus $a_{crit}$, $k_b$ is Boltzmann constant, and $T$ is temperature in K.

$$a_{crit} \cdot \frac{e \cdot V_g \cdot df}{d} = \frac{\hbar^2 \pi^2 N_i^2}{2 \cdot m_{eff} \cdot a_{crit}^2}$$  (2)

$$\rho_{max} = \frac{1}{d^2 \cdot a_{crit}(V_g) + d^2 \cdot \int_{0}^{a_{crit}(V_g)} \exp(-\frac{e \cdot V_g \cdot df}{d \cdot k_b \cdot T} \cdot x) \, dx}$$  (3)

The tunneling current is the product of the electron density at the bottom of the dot, density of states, thermal velocity, and tunnel probability. Equation 4 shows the case for positive gate bias where electron density decreases exponentially from top to bottom of dot as in first exponential term. $A$ is the area of the dot, $N_c$ is the density of states in Si normalized to 300K, $\phi_b$ is barrier height. An effective mass of 0.42$m_o$ [11] and barrier height of 3.2eV [12] are used for tunneling current calculation.

$$J_{un} = \rho_{max} \cdot \exp\left(-\frac{(d - a_{crit}) \cdot e \cdot V_g \cdot df}{d \cdot k_b \cdot T}\right) \left(A \cdot N_c \cdot T^{3/2}\right)^{1/2} \cdot \exp\left(-2 \left(\frac{2 \cdot m_{eff} \cdot e \cdot \phi_b}{\hbar^2} \right)^{1/2}\right) \cdot t_{on} \quad V_g > 0$$  (4)

Equation 5 describes tunnel current with negative gate bias since electrons are localized at the bottom of the dot at a density of $\rho_{max}$. In this case the electron distribution shown in Figure 5 is inverted and there is small influence from gate bias.

$$J_{un} = \rho_{max} \cdot \left(A \cdot N_c \cdot T^{3/2}\right)^{1/2} \cdot \exp\left(-2 \left(\frac{2 \cdot m_{eff} \cdot e \cdot \phi_b}{\hbar^2} \right)^{1/2}\right) \cdot t_{on} \quad V_g < 0$$  (5)

The experimental data of lifetime ($1/J_{un}$), with fits to the model are shown in Figure 6. The data for negative gate bias is collected from pulse sequence shown in Figure 4 while for positive gate bias emission times were measure directly from charging/discharging process at the given read bias. The fits to the model shown in Figure 6 only use dot size and tunnel oxide thickness as adjustable parameters, as they cannot be precisely determined experimentally. Each fit was
normalized to the longest measured lifetime by changing tunnel barrier thickness, while the various slopes are a result of different dot size. A dot size of 9nm best represents the observed data and is consistent with the physical diameter of deposited dots. Importantly the proposed model accounts for the relatively small gate bias dependence on memory lifetime and predicts two different slopes for positive and negative gate bias. In the case of positive gate bias, it is possible to decrease electron density at the channel side of dot by several orders of magnitude with applied bias. For 12nm diameter dots an upper limit for the ratio of erase to store time can be $10^3$ using the direct tunneling with electron polarization within dot model for memory lifetime. However a larger nc-Si dot results in a tradeoff of reduced threshold shift per electron. Thus the introduction of deep interfacial traps may be necessary to improve memory retention properties.

CONCLUSIONS

Memory devices sensitive to the charge of a single electron stored in a nc-Si have been successfully fabricated allowing for the study of charge storage mechanism. Temperature dependence of lifetime shows an absence of activation energy, thus charge storage in interfacial traps is not the primary mechanism of charge retention. By using RPECVD derived nc-Si it is possible have an electron delocalized over the entire dot. Similar behavior could be expected from other devices if processing insures good Si/SiO$_2$ interface with nc-Si. By using a model that accounts for the ability to localize charge at the top of the dot away from channel, the gate bias affect on lifetime is predicted by using a classical approach for electron density combined with a direct tunneling process. The authors would like to thank Amit Dutta and Katsuhiko Nishiguchi for aid with e-beam lithography. Funding provided by JSPS and CREST.

REFERENCES

10  Taurus 1999.1 Avant! Corp., 46871 Bayside Parkway, Fremont, CA 94538.